

US 20140035116A1

(19) United States

(12) Patent Application Publication Xue et al.

(10) Pub. No.: US 2014/0035116 A1

(43) **Pub. Date:** Feb. 6, 2014

(54) TOP EXPOSED SEMICONDUCTOR CHIP PACKAGE

- (71) Applicant: **Alpha and Omega Semiconductor Incorporated**, Sunnyvale, CA (US)
- (72) Inventors: Yan Xun Xue, Los Gatos, CA (US);
 Yueh-Se Ho, Sunnyvale, CA (US);
 Hamza Yilmaz, Saratoga, CA (US);
 Anup Bhalla, Santa Clara, CA (US);
 Jun Lu, San Jose, CA (US); Kai Liu,
 Mountain View, CA (US)
- (73) Assignee: Alpha and Omega Semiconductor Incorporated, Sunnyvale, CA (US)
- (21) Appl. No.: 14/056,047
- (22) Filed: Oct. 17, 2013

Related U.S. Application Data

(62) Division of application No. 12/968,159, filed on Dec. 14, 2010, now Pat. No. 8,586,414.

Publication Classification

- (51) **Int. Cl. H01L 23/495** (2006.01)

(57) ABSTRACT

A semiconductor package and it manufacturing method includes a lead frame having a die pad, and a source lead with substantially a V groove disposed on a top surface. A semiconductor chip disposed on the die pad. A metal plate connected to a top surface electrode of the chip having a bent extension terminated in the V groove in contact with at least one of the V groove sidewalls.

